

## THE CDF LAYER 00 DETECTOR

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The CDF Layer 00 detector consists of single-sided silicon sensors assembled on the beampipe, forming the innermost of eight silicon layers in the CDF detector for Run II of the Fermilab Tevatron. Radiation tolerant p-in-n silicon with 25(50)  $\mu\text{m}$  implant(readout) pitch are mounted on a lightweight, cooled support structure and connect to electronics outside the tracking volume via long, fine-pitch cables. Layer 00 will significantly improve the impact parameter resolution and enhance the longevity of the silicon system, benefitting a large portion of the physics program for Run II.

### 1. Introduction

The heart of the CDF silicon system for run two of the Fermilab Tevatron, the SVXII, is a significant upgrade from the previous SVX'.<sup>1</sup> However, there are still performance-limiting weaknesses in the design of SVXII. First, the electronics and associated cooling are inside the tracking volume, significantly degrading impact parameter resolution for low-momentum tracks over a third of the SVXII coverage. Second, having been designed before the advent of radiation-tolerant silicon developed for the LHC, the lifetime of the critical innermost layer (layer 0) is expected to be only  $5 \text{ fb}^{-1}$ . Finally, all five layers of SVXII must be disassembled in order to replace the innermost layers, making upgrades for an extended Run II difficult and time-consuming. The Layer 00 silicon detector was proposed to address these shortcomings. Placing a lightweight layer of radiation-tolerant silicon directly on the beampipe greatly improves the impact parameter resolution for low-momentum tracks and extends the useful lifetime of SVXII beyond the failure of layer 0. Such a device is relatively simple to replace in a short period of time.

### 2. Design

The constraints on the design of Layer 00 are severe. It must fit between the beampipe ( $r=1.25 \text{ cm}$ ) and the inner bore of SVXII ( $r=2.1 \text{ cm}$ ). To meet the goal of lasting  $>5\text{-}10 \text{ fb}^{-1}$ , it must withstand 5-10 MRad, requiring radiation-tolerant silicon. This silicon must be cooled to remove heat due to the ambient environment ( $\approx 15 \text{ W}$ ) as well as that due to leakage currents after irradiation ( $\approx 15 \text{ W}$ ). Material must be minimized to best benefit low-momentum tracking. With limited time and resources available, standard SVXII DAQ must be used. Inclusion of Layer 00 in the dead-timeless Silicon Vertexing Trigger (SVT) allows only certain geometries and requires alignment of  $\approx 100 \mu\text{rad}$  between the  $\phi$ -strips of Layer 00 and SVXII.

The design has six narrow (128 channel) and six wide (256 channel) groups in  $\phi$  at  $r = 1.35$  cm and  $r = 1.62$  cm respectively. There are six readout modules in  $z$ , with two sensors bonded together in each module for a total length of 95 cm. The sensors are mounted on a carbon-fiber support structure with integrated cooling. To save space, eliminate material and protect the readout chips from radiation, the hybrid circuit boards containing the front-end electronics (13,824 channels) are mounted on separate cooling structures beyond the ends of the silicon. The sensors are connected to the readout chips via long fine-pitch signal cables.

The sensors are single-sided p-in-n  $\langle 100 \rangle$  silicon with a  $25(50)$   $\mu\text{m}$  implant(readout) pitch. These have been produced by Hamamatsu Photonics (HPK), SGS-Thompson (ST) and Micron. Micron has also produced oxygenated sensors for Layer 00. The addition of intermediate strips that are not read out improves spatial resolution down to  $S/N=6$  without significant degradation in efficiency or two-hit separation. These sensors typically hold 700-1000 volts before breakdown, allowing full depletion after high radiation doses. The wide groups will be produced using only HPK sensors, while the narrow groups will be comprised of five  $\phi$ -wedges of ST sensors and one  $\phi$ -wedge of oxygenated Micron sensors. Figure 1 shows a pair of sensor modules attached to their fine-pitch readout cables.

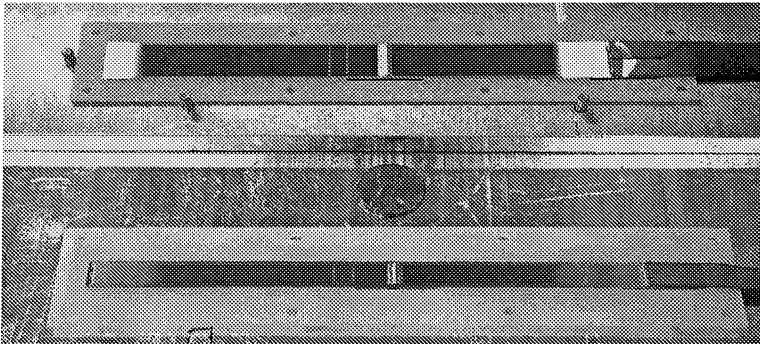


Fig. 1. Wide(top) and narrow(bottom) sensor modules with a US penny for scale.

The carbon fiber supports are comprised of three layers. The outermost utilizes a  $0^\circ$ - $90^\circ$  layup of unidirectional fibers to achieve the necessary thermal conductivity while allowing the sharp corners required. The middle layer uses unidirectional fiber to transport heat circumferentially to four integrated cooling passages containing 2mm thin-walled aluminum tubing. The innermost layer utilizes a carbon fiber weave to make the whole more robust. The three layers are cold-bonded to form a complete shell and four of these shells are joined around the beampipe to make the complete structure. Tests indicate that the warmest sensors will operate at roughly  $-2^\circ\text{C}$  before irradiation and  $4^\circ\text{C}$  after  $5\text{ fb}^{-1}$ . Even running at a constant  $5^\circ\text{C}$ , Layer 00 is expected to last at least  $7.4\text{ fb}^{-1}$ .

The lightweight fine-pitch cables are fabricated on 50  $\mu\text{m}$  thick polyimide film at CERN.<sup>2</sup> The traces are 1-1.5  $\mu\text{m}$  of gold atop 5  $\mu\text{m}$  of copper and are 10-12  $\mu\text{m}$  wide. The 50  $\mu\text{m}$  pitch (0.47 pf/cm) at the silicon and hybrid ends fans out to 100  $\mu\text{m}$  (0.33 pf/cm) over most of the length to reduce capacitance. The longest cable is 47 cm with a capacitance of  $\approx 17$  pf.

The front end electronics consist of SVX3d chips on single-sided alumina hybrid circuit boards.<sup>3</sup> Three narrow sensor modules connect to a single three-chip hybrid while each wide module connects to a two-chip hybrid. The hybrids are mounted on cone-shaped carbon-fiber cooling structures beyond the ends of the silicon that place the chips at the largest possible radius to reduce radiation exposure. All other DAQ is standard SVXII DAQ with the exception of HV supplies: all Layer 00 components are tested to 500V. Despite higher physics occupancy, readout times are smaller than that for SVXII due to the small number of total channels.

### 3. Performance and Physics Impact

The performance of Layer 00 modules is roughly as expected: the noise agrees with predictions, the pedestals are relatively flat and common mode noise from pickup on the signal cables is almost entirely environmental. Although common-mode noise is negligible in a shielded environment, the dynamic pedestal subtraction (DPS) feature of the SVX3d chip will be used to remove any which may be present when installed on the beampipe inside of SVXII. With DPS enabled, the expected S/N distribution for Layer 00 ranges from 9-12 at the beginning and 8-11 after  $5 \text{ fb}^{-1}$ , including the effects of different cable lengths and radii of readout chips. Because the intermediate strips improve single-hit resolution significantly in this range of S/N, adjustments are made wherever possible (e.g. maximizing the SVX3d amplifier current) to better noise performance. Single-hit resolutions of 6-9  $\mu\text{m}$  and efficiencies of 93-98% in the entirety of Layer 00 for at least  $5 \text{ fb}^{-1}$  are expected.

The most obvious benefits of Layer 00 are for low- $p_t$  physics. More displaced tracks are found, improving  $b$ -tagging, while better impact parameter resolution further enhances the reach of CDF for studies of  $B_s$  mixing and CP violation. With 50% of  $b$ -daughter tracks in top decay having  $p_t < 3 \text{ GeV}$ , Layer 00 will also benefit high- $p_t$  physics by increasing the tagging efficiency for  $b$ -jets in top and Higgs events. Improved measurement of the displaced-track multiplicity may help distinguish  $b$  and  $c$  decays and better impact parameter resolution may even allow tertiary charm vertexes to be distinguished from secondary  $b$ -vertexes.

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2. A. Gandi, CERN Microcable group.
3. M. Garcia-Sciveres *et al.*, *Nucl. Instr. and Meth. A* 435 (1999), pp.58-64.