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# Proposal for Intermediate Silicon Layers in CDF

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**Abstract**

The CDF SVXII silicon detector will provide coverage to $|\eta| < 2$. In the region $|\eta| < 1$ the combination of the SVXII detector and the Central Open Cell Tracker (COT) will yield precise 3D tracking with high efficiency and purity. For $|\eta| > 1$, it may be possible to perform 2D tracking with SVXII alone but, in the absence of larger radius hit information, the impact parameter resolution for such tracks will be too poor to enable efficient b tagging. The 4 layer Intermediate Fiber Tracker (IFT) would alleviate this problem for run II. An alternative possibility of comparable cost would be the installation of a small number of intermediate radius layers of double-sided silicon strip detectors similar to layers 2 and 4 of SVXII. In this note we describe the option of Intermediate Silicon Layers (ISL) in detail. It is comparable to the IFT in cost and would duplicate most of that detector's intended functions including useful operation in run III (TeV33), while also providing a number of advantages.

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# 1 Introduction

In this note we present a silicon strip solution to CDF's need for intermediate radius tracking information in runs II and III. In arriving at the detailed solution we present here, our goals have been to:

- Extend pseudorapidity coverage to $|\eta| \sim 2$ for good acceptance of b jets from top and light Higgs decays, and forward leptons.
- Make measurements at large enough radii and with sufficiently good hit resolution to obtain good momentum and impact parameter resolution.
- Design the detector such that it can be built rapidly and robustly.
- Reduce cost by minimizing the number of readout channels per unit area of silicon.
- Retain the $30^o$ wedge structure of SVXII to leave open the option of including the detector in a future extension of the Silicon Vertex Trigger (SVT).
- Minimize any burden on the SVXII group and make available additional manpower for the completion of the silicon detectors.

For Si microvertex detectors many of these goals are contradictory. Many difficult tasks associated with the construction of a microvertex detector are however eliminated at larger radii. For example, the occupancy is lower and radiation damage occurs more slowly. This means that it is possible to use longer strips and wider readout pitch to reduce the number of readout channels and subsequent cost of front-end electronics and Data Acquisition (DAQ). In addition, the intermediate radius region of CDF is rather spacious. This added real estate can be used to obtain a mechanical design for which the actual construction of the detector is more simple and robust while also less costly. Finally, since the layers are further from the interaction point, it can be demonstrated that construction tolerances are slightly more relaxed which again affords an opportunity to streamline the construction of the device.

With these goals and opportunities in mind we have arrived at a workable and fairly detailed solution. The concepts we present were developed over

a span of only 3 weeks and the designs were produced over a period of several days. We therefore consider this to be a "worked example" for which small refinements and optimizations may still occur. Such alterations would however only be made if they further simplify the construction and reduce the cost of the device. The costs and schedule we present for the current design are therefore believed to be realistic.

# 2 Overview of the Detector Design

The various silicon layers proposed in our baseline design are shown in Figure 1. These lie within the radial range $20 < r < 30$ cm and extend to $|z| = 65$ cm for the inner layer and 87.5 cm for the outer layer ($|\eta| \sim 1.9$ in both cases). Figure 2 shows the end view of the two layers at large $\eta$ with the various radial positions of the silicon indicated.

All ladders will be identical and will be made from 3 crystals laid end to end. Each crystal measures 58 mm wide by 74 mm long so that two crystals can be made on a single 6 inch Si wafer. The crystals will be double-sided with axial strips on one side and small angle stereo strips on the other. The stereo angle is $1.2^o$. On both sides, the readout pitch (RP) will be twice the strip pitch (SP). The axial (p implant) side will have a SP $= 55\ \mu m$ yielding a hit resolution of better than 16 $\mu m$. The stereo (n implant) side will have SP $= 73\ \mu m$ yielding a hit resolution perpendicular to the strip direction of better than 23 $\mu m$. The specifications and performance characteristics for several other Si detectors of this type are compared to our proposal in the table below.

| | Atlas | Atlas | L3 | L3 | Delphi | Delphi | ISL | ISL |
|---|---|---|---|---|---|---|---|---|
| side | n | n | p | n | n | n | p | n |
| S/N | 11 | 17 | 15 | 15 | 12 | 21 | >12 | 12 |
| RP ($\mu m$) | 112 | 112 | 50 | 150 | 100 | 50 | 110 | 146 |
| SP ($\mu m$) | 56 | 56 | 25 | 50 | 100 | 50 | 55 | 73 |
| SP/$\sqrt{12}$ | 16.0 | 16 | 7.2 | 14.4 | 28.0 | 14.4 | 16.0 | 21.0 |
| $\sigma$ ($\mu m$) | 15.6 | 12.9 | 7.0 | 15.0 | 23.0 | 10.0 | <16.0 | <23.0 |

The readout hybrid ("ear") will be double sided ceramic (alumina or BeO) with 4 (3) SVX3 readout chips on the axial (stereo) side which are

matched to the detector strips by means of a pitch adaptor. Figure 3 shows the stereo side of a barrel 'slat' which is made up of two readout ladders containing 3 crystals each. Figures 4 and 5 show close up views of the $z$ and $\phi$ readout segments. On the $\phi$ side is shown the attachment of the ceramic to a Be block by means of 'ear-pins' like those used to attach ladders to the Be bulkheads in the CDF SVX and SVX′ detectors. The Be block contains a water cooling channel for which the entrance and exit pipes are shown near the ends of the block and the cover for the channel is seen on the top of the block. The size of the cooling channel is $3.5 \times 3.5\ mm^2$ which was determined by comparison to the SVXII design. It is expected to be more than adequate for maintaining the hybrid at desired operating temperatures. An important design feature of the ladder is the positioning of the C-fiber and foam support rails. As seen in the figure, the main support rails running the length of the ladder do not overlap any part of the silicon crystals. The crystals are instead supported by 'rungs' which bridge the main rails. This 'outrigger' design differs from the SVXII ladder design and results in open access to all bonding pads on both sides of the Si crystals. Another difference from the SVXII design is that the readout hybrids are not glued to the silicon, but are placed at the ends as in the SVX and SVX′ designs. Since the hybrids do not lie directly on the Si wafers, the transfer of heat to the Si is determined by the thermal pathways provided by the microbond wires. Heating of the Si itself is thus less of a problem than for SVXII. These two features can be achieved without introducing dead areas in the layers by taking advantage of the large amount of space available at large radii. The result is a simple and robust ladder design which can be fabricated more safely and rapidly than the SVXII ladder design.

Ladders will be supported by C-fiber disks. Note that in the larger radius layer, three ladders are attached to a single cooling channel per $30^o$ wedge. A closeup is shown in Figure 6. The central ladder is attached to one side of the block and the outer two are on the opposite side. This allows adjacent ladders to be overlapped. The overlap in the design shown is $\sim$6 mm. For the inner radius layer we show alternate 3 ladder and 1 ladder wedges. This is one simple way of constructing the layer which however does not strictly conserve $30^o$ rotational symmetry. In practice, we will likely use a scheme involving two ladders per cooling channel which would respect the $30^o$ wedge structure. In any case, there is a fair amount of flexibility in choosing the final layout.

Figure 7 shows the basic layout of the C-fiber support disks. Oblong channels would allow the passage of cables. Smaller holes are shown for cooling pipes and the attachment and alignment pins. Three sets of holes at $120^o$ spacings would enable the two layers to be referenced and connected by means of additional disks which would attach to C-fiber cylindrical shells. A cross sectional view (r-z plane) of the endplug barrel with offset layers is shown in Figure 8. A closeup view of the connection of the two layers is shown in Figure 9.

# 3 Necessary and Achievable Tolerances

The most crucial aspect of the construction of the detector is the ladder internal alignment. By this we mean the alignment of strips from wafer to wafer and the referencing of the strips to the ear-pin holes on the readout hybrid. Ideally one would like this alignment to be better than the intrinsic hit resolution of the Si. Fortunately the construction of the ladder is carried out with a precision coordinate measuring machine (CMM) having typical resolution of 0.1-0.2 mil (2.5-5.0$\mu m$) using positioning fixtures like those used in the SVX and SVX$'$ projects. In the SVX projects, the ladder internal alignments that were achieved were consistent with the CMM resolution.

Ladder to ladder alignments in a given layer, from layer to layer, and relative to the SVXII ladders are important for the pattern recognition but do not necessarily limit the final resolution of the device. In particular, it is anticipated that the ladders will be aligned using tracks which traverse the COT and SVXII. Thus, given that the ladders are themselves very precisely constructed, it should be possible to locate them and determine alignment constants that describe how their positions deviate from nominal. This will insure that hit resolution is not degraded for those cases in which the z locations of the axial hits are known. The latter is necessary in order to remove $r\phi$ displacements resulting from strips not being parallel to those in SVXII. We have chosen $\pm 75$ $\mu m$ as our specification for tolerable $r\phi$ ladder-to-ladder misalignment (in a single layer) to insure the convergence of the alignment procedure. As discussed below, the actual misalignments are expected to be about half this amount.

If the pattern recognition relies on starting from axial-only reconstruction of tracks in Si layers, then the z location of axial hits will not yet be known

and the actual relative misalignments of ladders will contribute an $r\phi$ uncertainty which could be large. Ideally, you want the maximum $r\phi$ deflection relative to SVXII ladders to be less than the two hit resolution ($\sigma = 220\mu m$) and less than the $r\phi$ pointing resolution from SVXII ($\sigma = 250\mu m$). It can be shown that this means that the deflection angle $\delta\alpha$ which measures the degree to which the strips in an outer layer are not parallel to those in SVXII, should satisfy

$$\delta\alpha < \frac{2\sigma}{L(1.5 + \frac{1.0}{\sqrt{12}})} = 0.4 \ \ mrad$$

Note that this corresponds to 8 mil across the $L \sim 50$ cm length of the barrel. It is our plan to build the intermediate radius Si layers directly onto the SVXII spaceframe using a large CMM for alignment. This will allow the relative angle between the axis of SVXII and that of the ISL layers to be kept to $\delta\alpha < 0.20\ mrad$. This is adequate to allow axial-only tracking provided the ladder to ladder alignment in the ISL is not itself worse than 8 mil.

The ladder to ladder $r\phi$ alignment within the ISL is determined by several factors. First, the alignment of the hybrid connection holes to the pin holes on the cooling block which attach the ladder to the C-fiber support disk will introduce an uncertainty of no more than 0.5 mil at each hybrid. The alignment of the Be block to the C-fiber support disk is dominated by the reference hole positioning and clearance. This can be achieved with an uncertainty of less than 1.0 mil at each end. Taking the conservative estimate for the ladder internal alignment to be $\pm 10\ \mu m$, it then follows that the ladder to ladder alignment in a single layer will be

$$\sigma < \sqrt{2 \cdot (10^2 + 13^2 + 25^2)} \sim 40\mu m$$

Layer to layer alignment will contribute an additional global uncertainty of 25-50 $\mu m$ which however will not seriously impact tracking alignment or ultimate performance of the detector. We conclude that the design we have presented will easily allow construction within the tolerances necessary for the success of the axial-only stage of the pattern recognition and for the alignment and full resolving power of the detectors in 3D tracking. A summary of the necessary and achievable tolerances is contained in the table below.

| | Necessary | Achievable |
|---|---|---|
| Wafer-to-Wafer | $\pm 5\ \mu m$ | $\pm 2.5\ \mu m$ |
| Wafer-to-Hybrid | $\pm 5\ \mu m$ | $\pm 2.5\ \mu m$ |
| Hybrid-to-Block | $\pm 13\ \mu m$ | $\pm 13\ \mu m$ |
| Block-to-Disk | $\pm 25\ \mu m$ | $\pm 25\ \mu m$ |
| Ladder-to-Ladder | $\pm 75\ \mu m$ | $\pm 40\ \mu m$ |
| ISL-to-SVXII | $\pm 200\ \mu m$ | $\pm 100\ \mu m$ |

# 4 Readout and Data Acquisition

SVX3 readout chips are used so that the data acquisition system is identical to SVXII. Each SVXII portcard has five inputs, one for each ladder in an SVXII wedge. Each input can address up to 14 chips. We will attach two ladders to each portcard input. This allows a single portcard to readout the five ladders in each of two $30^{\circ}$ wedges and reduces the size and cost of the DAQ system. Although, this assigns more channels to each portcard than is done in SVXII, the readout time for each portcard will still be less than SVXII since less $\eta\phi$ space is covered by each portcard input.

For the single layer located in the central region, the ladders can also be arranged into 60 degree wedges at larger radius to simplify the overlapping of the central and forward silicon. Again, two ladders are attached to each portcard input to reduce the DAQ cost while keeping the $\eta\phi$ readout segmentation smaller than in SVXII.

The component count for the ISL is compared to SVXII in the following table. Notice that the ISL uses more silicon than SVXII, but it has about half as many channels and portcards.

| | SVXII | ISL Plug | ISL Plug+Central |
|---|---|---|---|
| Detectors | 720 | 720 | 900 |
| Half ladders | 360 | 240 | 300 |
| Chips | 3168 | 1680 | 2100 |
| Channels | 405,504 | 215,040 | 268,800 |
| Hybrids | 720 | 240 | 300 |
| Port Cards | 72 | 24 | 30 |

# 5 Acceptance

By staggering the ladder radii, complete $\phi$ coverage is obtained. The $\eta$ coverage is $|\eta| < 1.9$. The effect of the extended luminous region, $\sigma_z = 30$ cm, is shown in Fig. 10. The 50% acceptance point is at $|\eta| \sim 2$.

# 6 Occupancy

The ISL occupancy will of course be very low. To estimate the occupancy in a $t\bar{t}$ event at a luminosity of $2 \times 10^{32}$, we measure the occupancy from MC $t\bar{t}$ and add six times the occupancy measured from minimum bias data. It is important to measure the minimum bias occupancy from data since the MC is known to underestimate it. The $t\bar{t}$ occupancy is 0.25%. The minimum bias occupancy is measured from Run 1b minimum bias triggers which are required to have one and only one primary vertex. This vertex is required to be within $|z| < 3$ cm. For such events, layer 3 of SVX′ has the same $\eta$ coverage as the ISL. So, we count hits in that layer and project to the ISL radius. This gives an estimate of 0.073% per minimum bias interaction. At $2 \times 10^{32}$ and 396 ns bunch spacing, an average of 6 minimum bias interactions are expected per crossing, yielding 0.44% occupancy. Adding the top contribution, gives an estimate of about 0.7% occupancy. These occupancies include the fact that each hit typically fires two strips.

# 7 Material

Since the ISL is made from components similar to SVXII, the material can be estimated from the SVXII material budget [1]. The ladders amount to $\sim 0.5\%$ of a radiation length for the central barrel and $\sim 1\%$ in the forward barrels. The additional material from the hybrids, bulkheads, portcards, etc., amounts to 1% of a radiation length when averaged over the length of the detector.

# 8 Tracking Performance

In the available time, it was not possible to perform a complete study of the simulated tracking performance of the ISL. However, we have studied the tracking efficiency and purity using a version of the SVX′ standalone tracker which was modified to accommodate the 5 layers of SVXII and to find tracks which cross wedge and barrel boundaries. The efficiency for finding standalone SVXII $r\phi$ tracks with 4 or more hits is 92%. The dominant source of inefficiency is the gaps between the barrels in z. At large $|\eta|$, a track is not likely to pass through two such gaps, so the efficiency increases to 97.7% for $|\eta| > 1$.

The pattern recognition simply finds all 4 or 5 hit combinations, so the initial purity of the tracks is low. The average signal to background ratio is 1:5. For 4 hit tracks, it is 1:10 while for 5 hit tracks, it is 1:2. (The 4 hit purity increases by a factor of 2 when an impact parameter cut of 2 mm is applied.) Fake tracks are combinations of hits from several different tracks, so these hits are "shared" by two or more tracks. Using a pruning algorithm which discriminates against tracks with shared hits, the signal to background ratio was increased to 4.5:1 with an efficiency of $> 90\%$ (see Figs. 11 and 12). The resolutions obtained with SVXII standalone tracking are shown in Fig. 13, and a display of a sample event is shown in Fig. 14. The pruning algorithm was developed over only a few days and is not optimized. It demonstrates, however, that the SVXII can provide standalone tracking with good purity and efficiency.

In the central region, matching the SVXII tracks to COT tracks would provide additional fake rejection and improve the momentum resolution (and therefore the impact parameter resolution). In the plug region, this is accomplished by the two layers of the ISL. To demonstrate the rejection power of a sixth layer of silicon, each SVXII track was projected to $r = 20$ cm and the "nearest hit" was found. The "hits" were made by simply recording the intersection points of all OBSP particles with a circle at this radius. This is certainly not a complete way of simulating the hits, but it is reasonable since the detector resolution is completely negligible compared to the $> 200\mu m$ pointing uncertainty of the SVXII tracks at $r = 20$ cm. The "nearest" hit includes knowledge of the z readout segmentation of the SVXII and the ISL.

(Knowing which SVXII barrels[2] contain a track's hits reduces the number of ISL barrels which must be searched by about two thirds.) The nearest hit is the correct hit 95% of the time. Requiring that the distance from the track's projected intersection point to the nearest hit be less than 2.5 mm ($\sim 10\sigma$ for high $P_T$ tracks) improves the signal to background ratio to 12:1. This demonstrates the rejection power of a single layer of ISL. An optimized pattern recognition using the entire seven layer system will lead to improvements in both efficiency and rejection.

Given that the SVXII and ISL will produce highly efficient and pure tracking with minimal CPU, an added benefit of the integrated Si tracker is the possibility to use these tracks as an integral part of the overall track reconstruction with the COT. In studies performed for the tracking godparents review of the SVXII in Dec. 1994 [3] it was shown that a Si tracker with an outer layer at a radius of 20 cm would have very good pointing accuracy into tracking devices at larger radii. The table below shows these results for the $r\phi$ pointing accuracy of such a device at various radii and for various transverse momenta. For an outer layer at 30 cm, the values for radii greater than 30 cm in the table fall by a factor of $\sim$2.5.

| Radius | $P_T = 1\ GeV$ | $P_T = 3\ GeV$ | $P_T = 5\ GeV$ | $P_T = 10\ GeV$ |
|---|---|---|---|---|
| 30 cm | 500 $\mu m$ | 120 $\mu m$ | 90 $\mu m$ | 70 $\mu m$ |
| 60 cm | 4 $mm$ | 1 $mm$ | 700 $\mu m$ | 560 $\mu m$ |
| 80 cm | 1 $cm$ | 2 $mm$ | 1.6 $mm$ | 1.2 $mm$ |
| 100 cm | 20 $cm$ | 5 $mm$ | 3 $mm$ | 2.6 $mm$ |
| 130 cm | 36 $cm$ | 7 $mm$ | 5 $mm$ | 4 $mm$ |

# 9 Cost

The cost estimate is summarized in the table below. For reference, the contributions from the forward barrels are separated from those for the central barrel. The unit costs include contingency and are taken from the SVXII cost estimate [2] where appropriate. The quantities include spares allocated

[2]Here *barrel* refers to the six logical barrels not the three mechanical barrels.

as in the SVXII cost estimate. The spare allocation and average contingency are summarized in a subsequent table. The total cost without contingency is 4.5 M$.

| | unit cost (k$) | Forward quantity | Forward cost (k$) | Central quantity | Central cost (k$) | Total cost (k$) |
|---|---|---|---|---|---|---|
| Silicon wafers | 3.63 | 432 | 1568 | 108 | 392 | 1960 |
| Mask order | 50 | 1 | 50 | 0 | 0 | 50 |
| Prototypes | 34 | 1 | 34 | 0 | 0 | 34 |
| **Silicon total** | | | 1652 | | 392 | 2044 |
| Hybrids | 0.40 | 269 | 108 | 67 | 27 | 135 |
| Design and prototype | 10.4 | 6 | 62 | 0 | 0 | 62 |
| **Hybrids total** | | | 170 | | 27 | 197 |
| **Chips** | 0.356 | 2184 | 778 | 546 | 194 | 972 |
| **DAQ** | 36.6 | 24 | 878 | 6 | 220 | 1098 |
| Mech. Design | | | 156.0 | | 0 | 156.0 |
| Techs. | | | 195.0 | | 24.0 | 219.0 |
| Wire bonder | 132 | 1 | 132.0 | | 0 | 132.0 |
| Ladder Support | | | 19.2 | | 4.8 | 24.0 |
| Ladder Assembly | | | 52.0 | | 4.8 | 56.8 |
| Ladder Frames | | | 12.1 | | 3.0 | 15.1 |
| Bulkhead Fab | | | 160.0 | | 80.0 | 240.0 |
| Barrel Assembly | | | 21.7 | | 10.8 | 32.5 |
| Installation | | | 34.7 | | 17.3 | 52.0 |
| Support Structure | | | 56.4 | | 0 | 56.4 |
| Cooling/Gas System | | | 65.0 | | 32.5 | 97.5 |
| **Mechanical total** | | | 904 | | 178 | 1082 |
| | | | | | | |
| **Total** | | | 4382 | | 1011 | 5393 |

| | spares | <contingency> |
|---|---|---|
| Silicon wafers | 20% | 10% |
| Hybrids | 12% | 30% |
| Chips | 30% | 30% |
| DAQ | 15% | 25% |
| Mechanical | 25% | 25% |

It is worth noting that about half of the DAQ cost ($\sim$ 500 k$) is for items which are placed outside the detector. If required by funding profiles, it would be possible to stage this cost.

# 10 Schedule

The construction of this detector is simplified by the fact that it reuses most of the electronics and DAQ solutions already developed for the SVXII project. This alleviates the need for DAQ R&D. Only the hybrids and silicon masks need to be prototyped. Furthermore, the simplifications afforded by the large radius streamline the construction process. A schedule for design and construction is shown in Fig. 15.

# 11 Conclusion

We have presented a silicon strip solution to CDF's need for intermediate radius tracking in run II. The radiation tolerance and low occupancy of this system make it suitable for continued use in run III as well. The cost is comparable to the 4 layer Intermediate Fiber Tracker. The design is simple to construct and reuses existing technology to reduce cost, schedule, and technical risks.

# References

[1] R. Snider, presentation at SVXII meeting, July '96.

[2] J. Spalding, private communication.

[3] E. Chao, R. Culbertson, J. Incandela, and F.D. Snider Dec. 15, 1994 tracking godparents review and Jan. 21, 1995 CDF collaboration meeting.

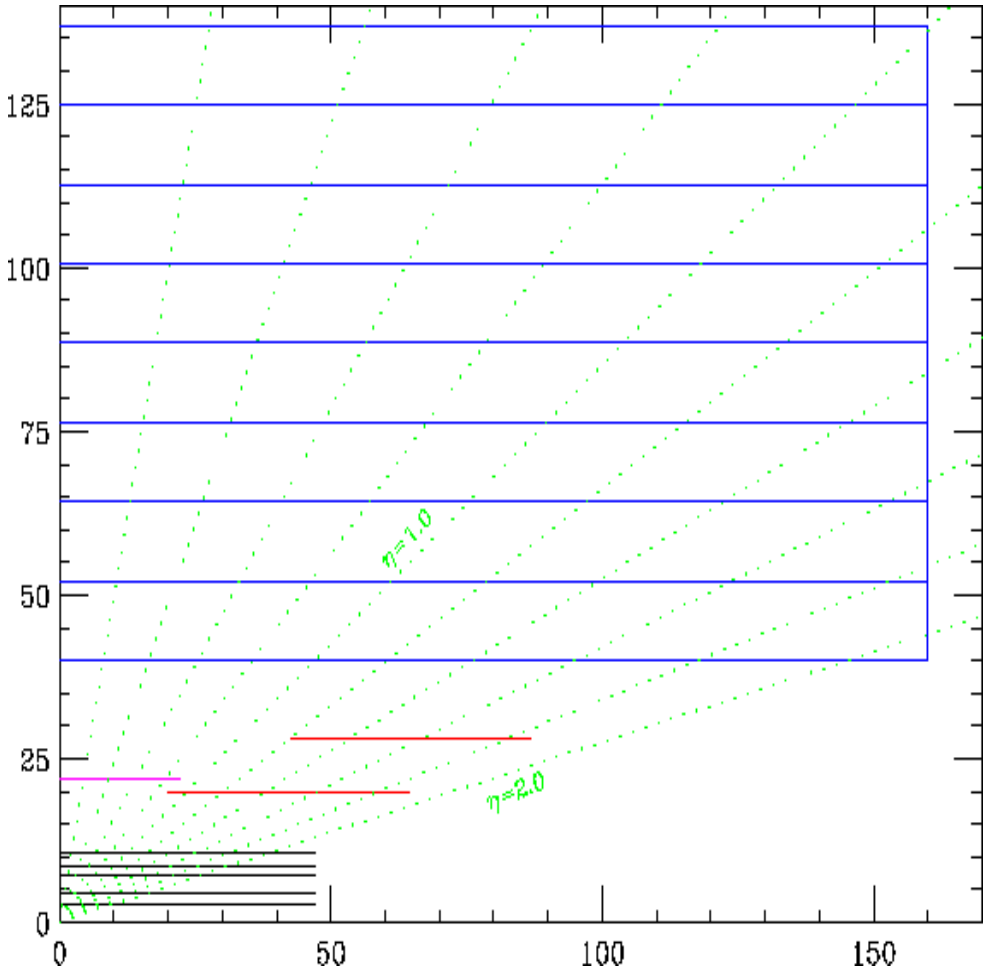


Figure 1: An r-z view of the proposed silicon layer placements. SVXII and COT are also shown.

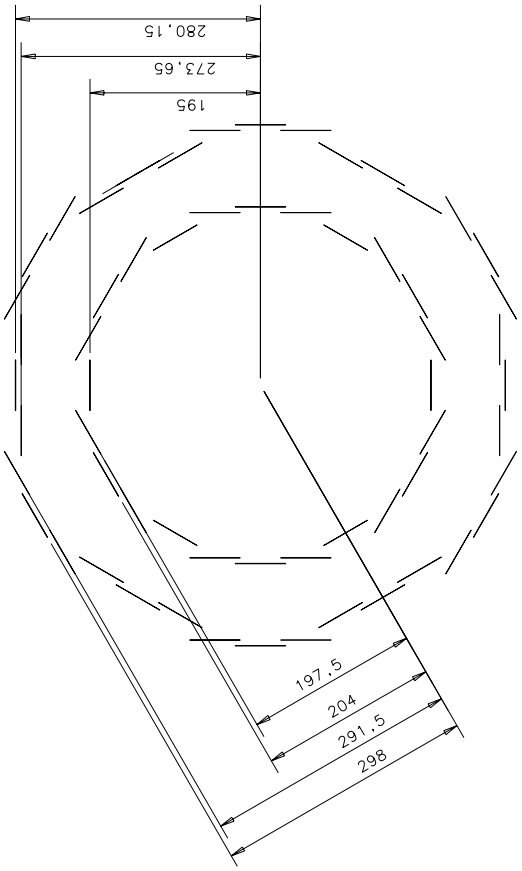




Figure 2: An r-$\phi$ view of the proposed silicon layer placements in the large $\eta$ region.

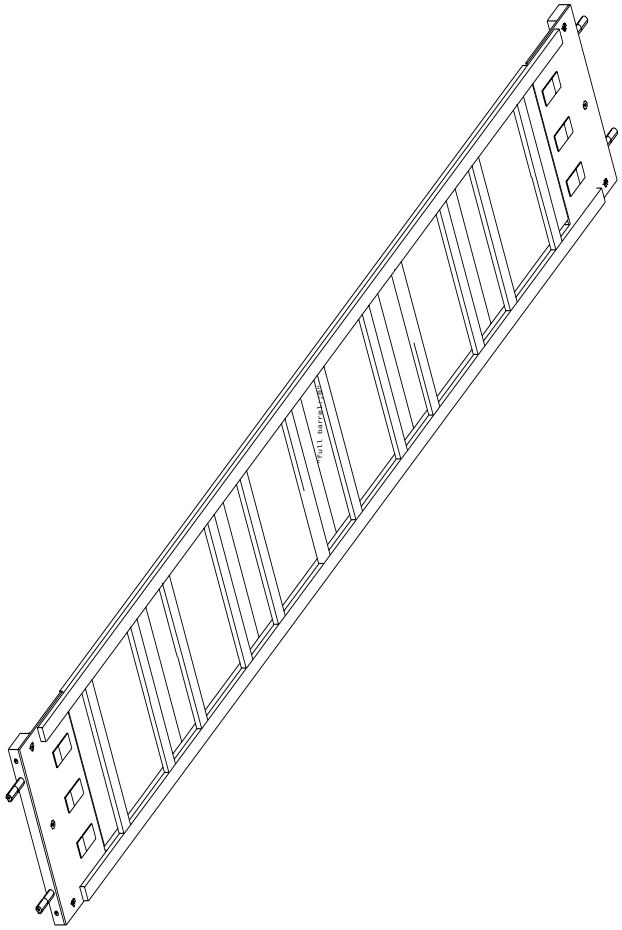

Figure 3: A view of the stereo side of a barrel 'slat' which consists of two ladders.

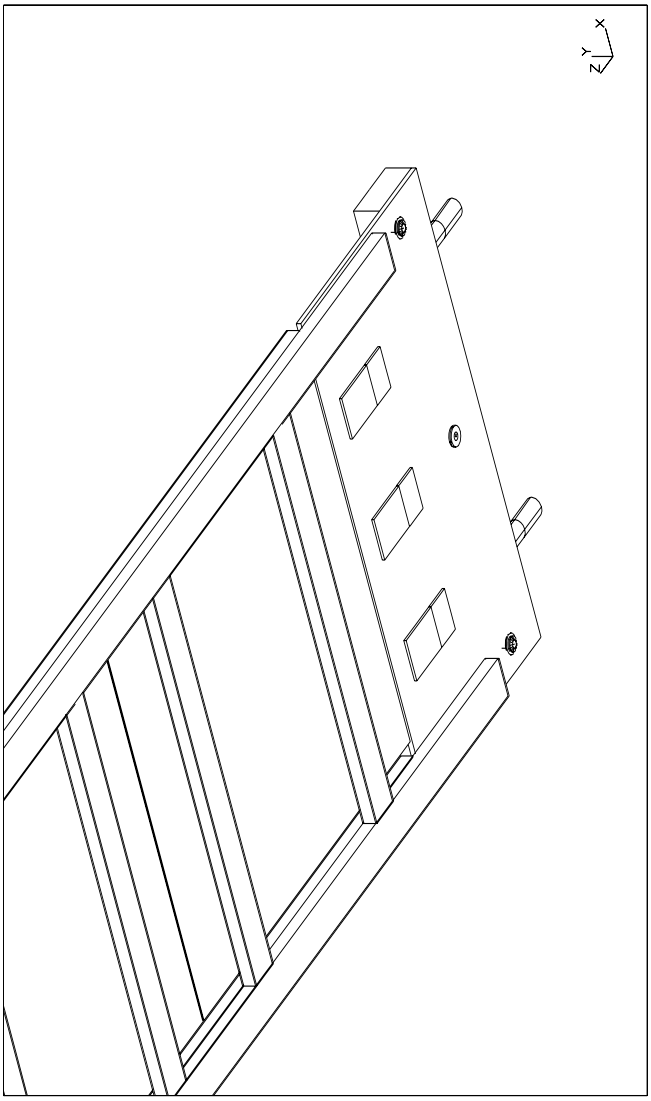


Figure 4: A close up view of the readout hybrid on the stereo side of a ladder.

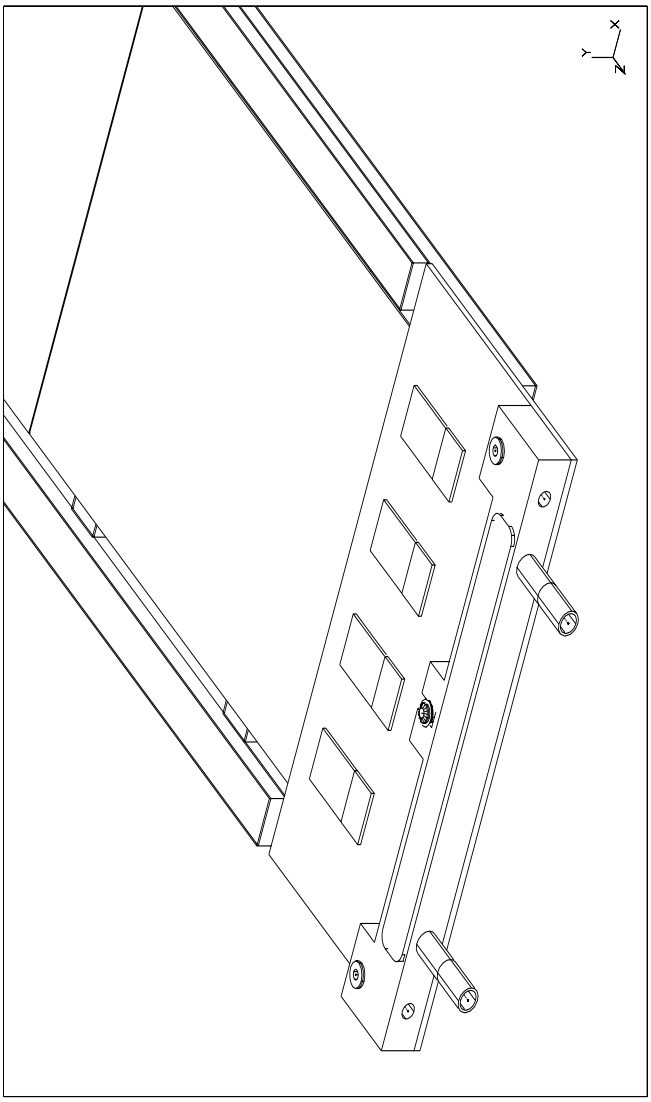

Figure 5: A close up view of the readout hybrid and cooling channel on the axial side of a ladder.

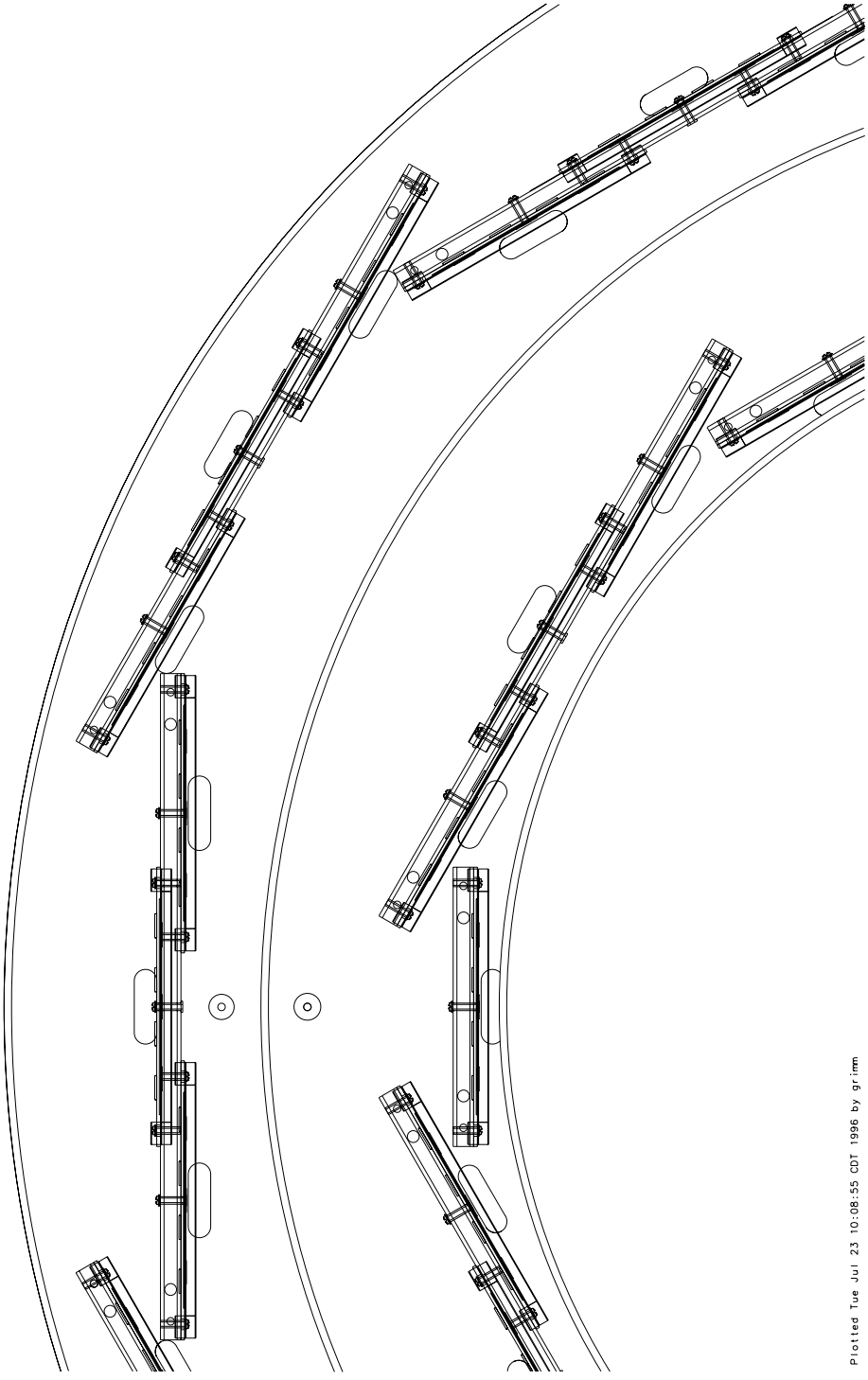


Figure 6: Closeup of one section of the endview of an endplug barrel.

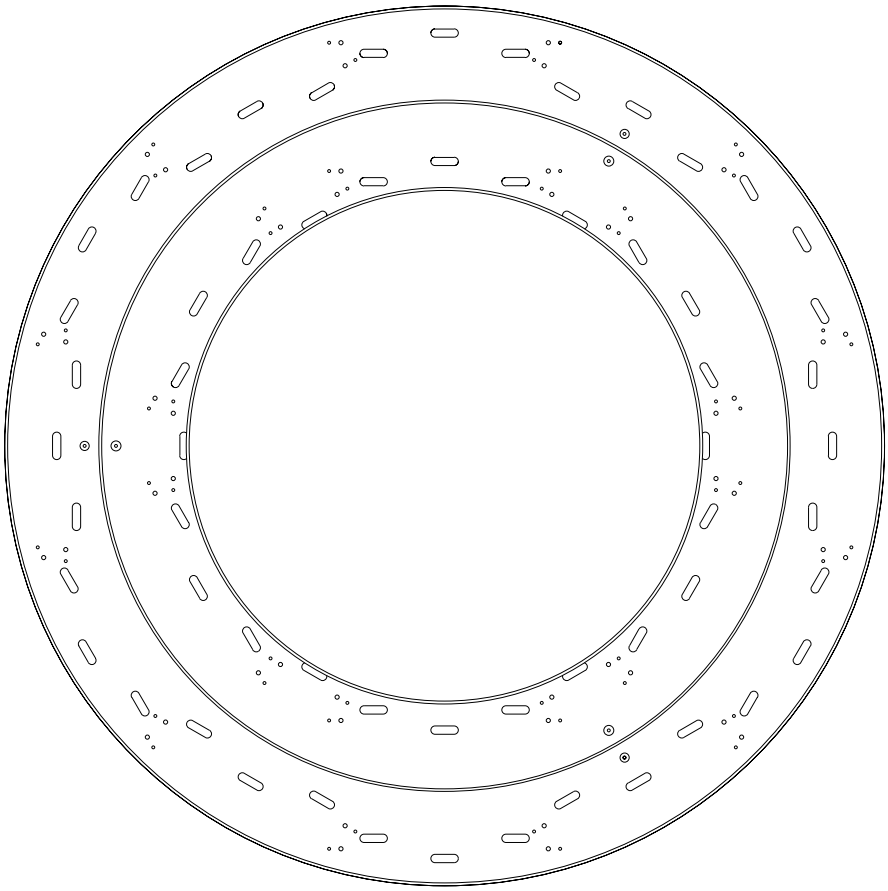

Figure 7: C-fiber support disks.

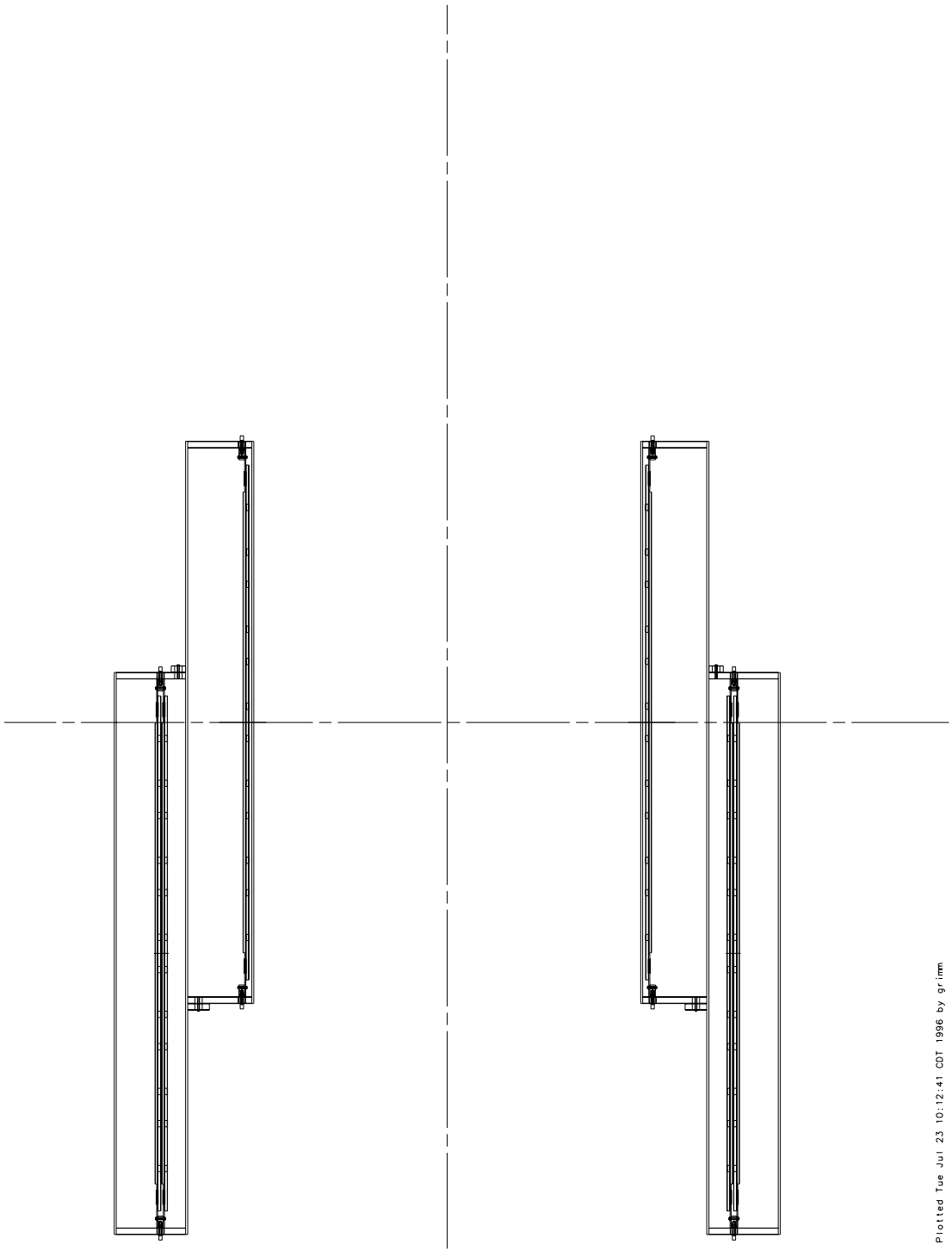


Figure 8: Endplug barrel side view (beamline is vertical in this view).

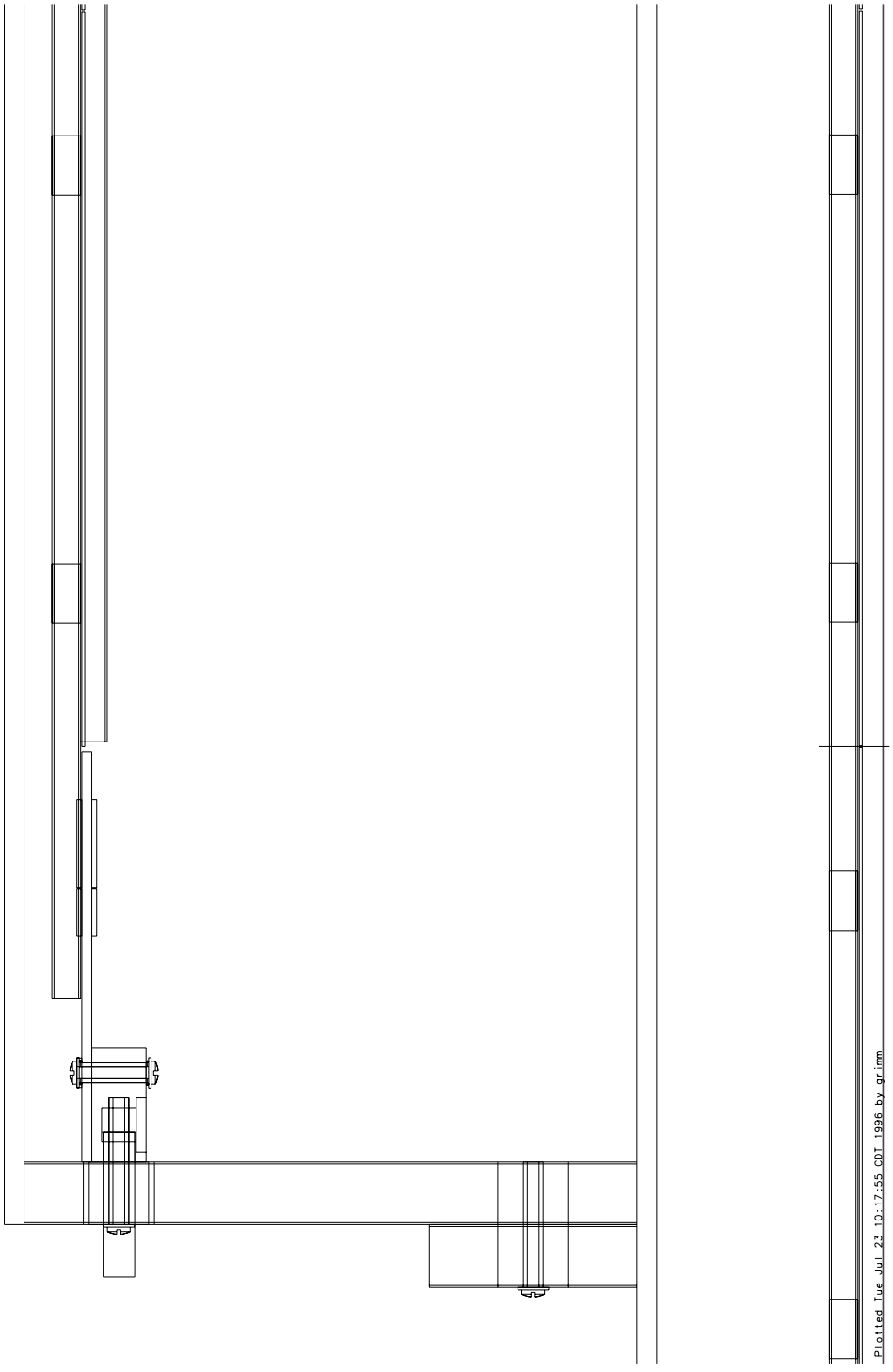


Figure 9: Closeup of layer connection in the endplug barrel.

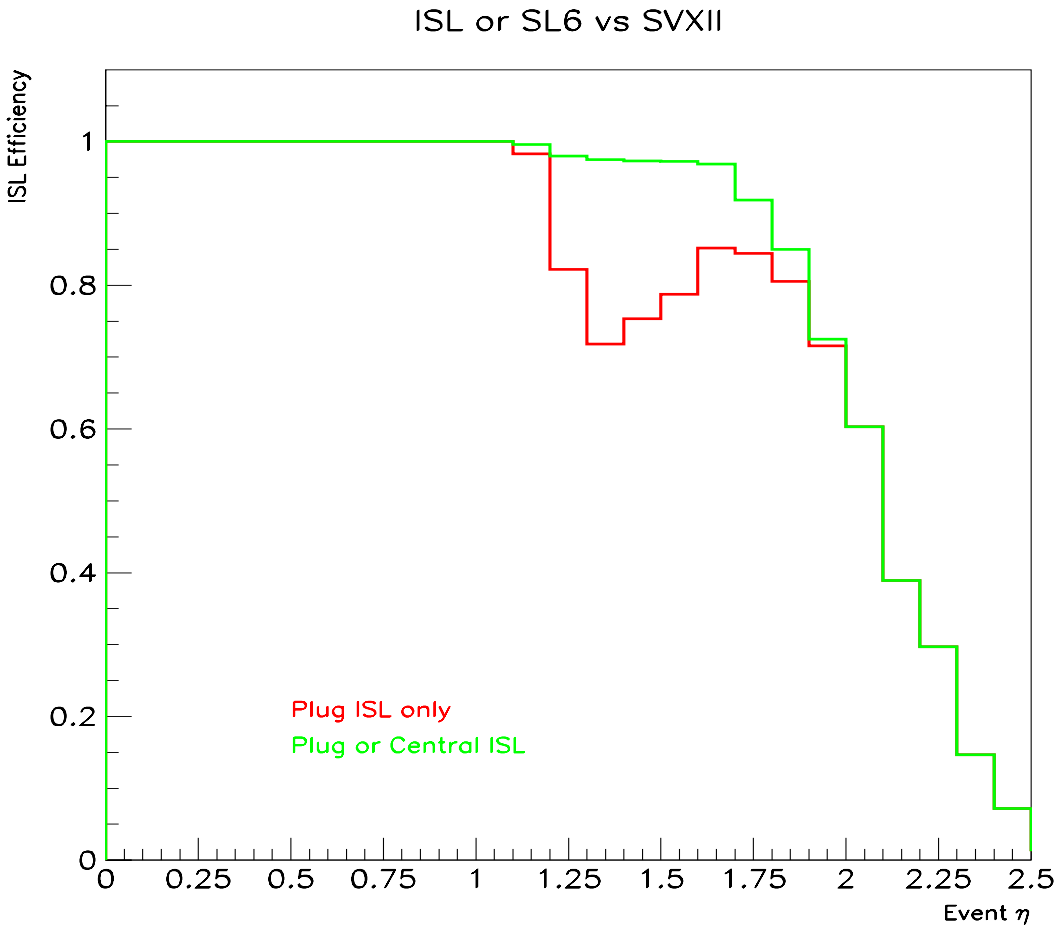


Figure 10: Acceptance as a function of "event" $\eta$, including the effect of the extended luminous region. The green (top) histogram shows the acceptance for particles which are in SVXII to also be in either the forward or central barrels of ISL. The red histogram shows the acceptance for particles which are in SVXII to also be in either the forward barrels of ISL or in SL6 of the COT. The dip in acceptance between 1.1 and 1.8 indicates the acceptance gain afforded by the central barrel of ISL.

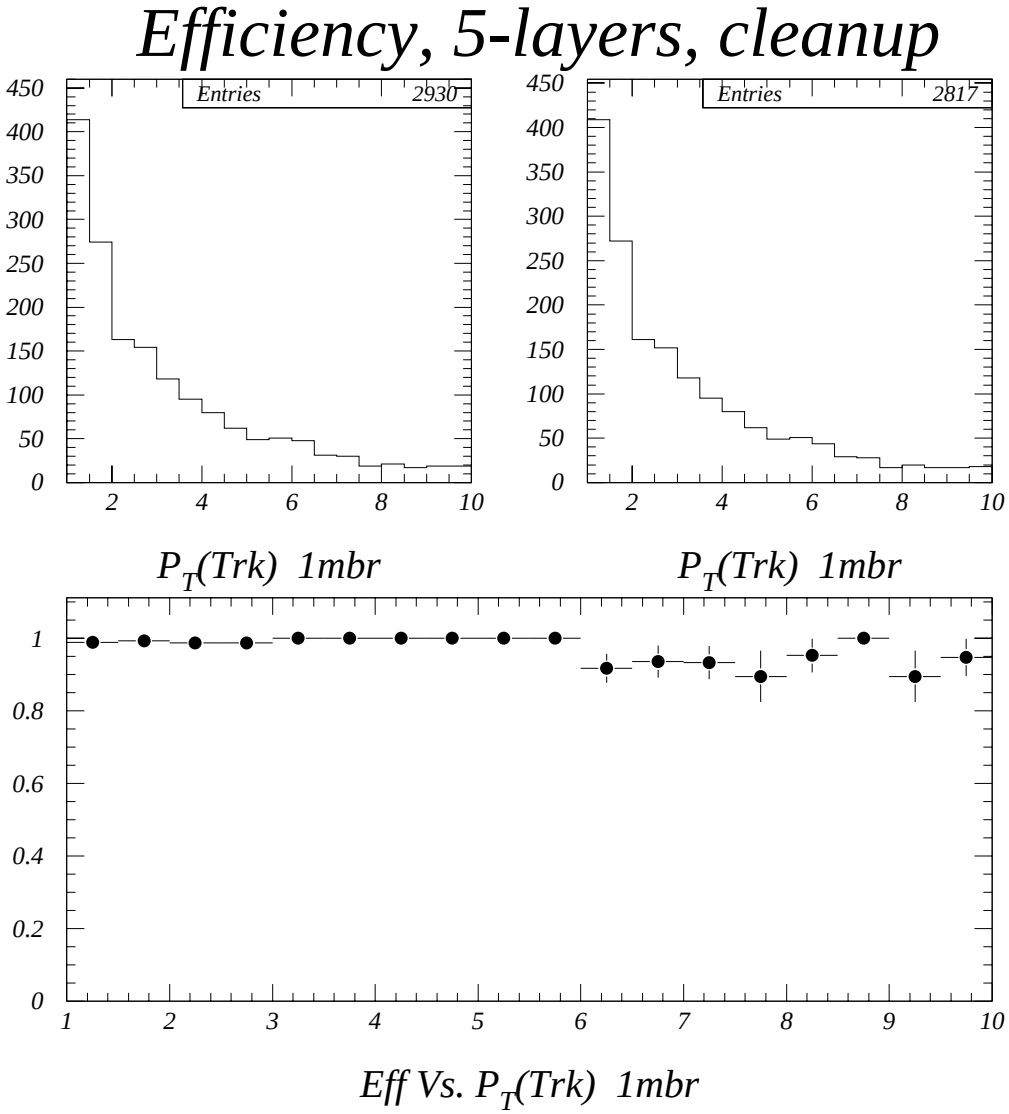


Figure 11: The efficiency of the SVXII pruning as a function of $p_T$.

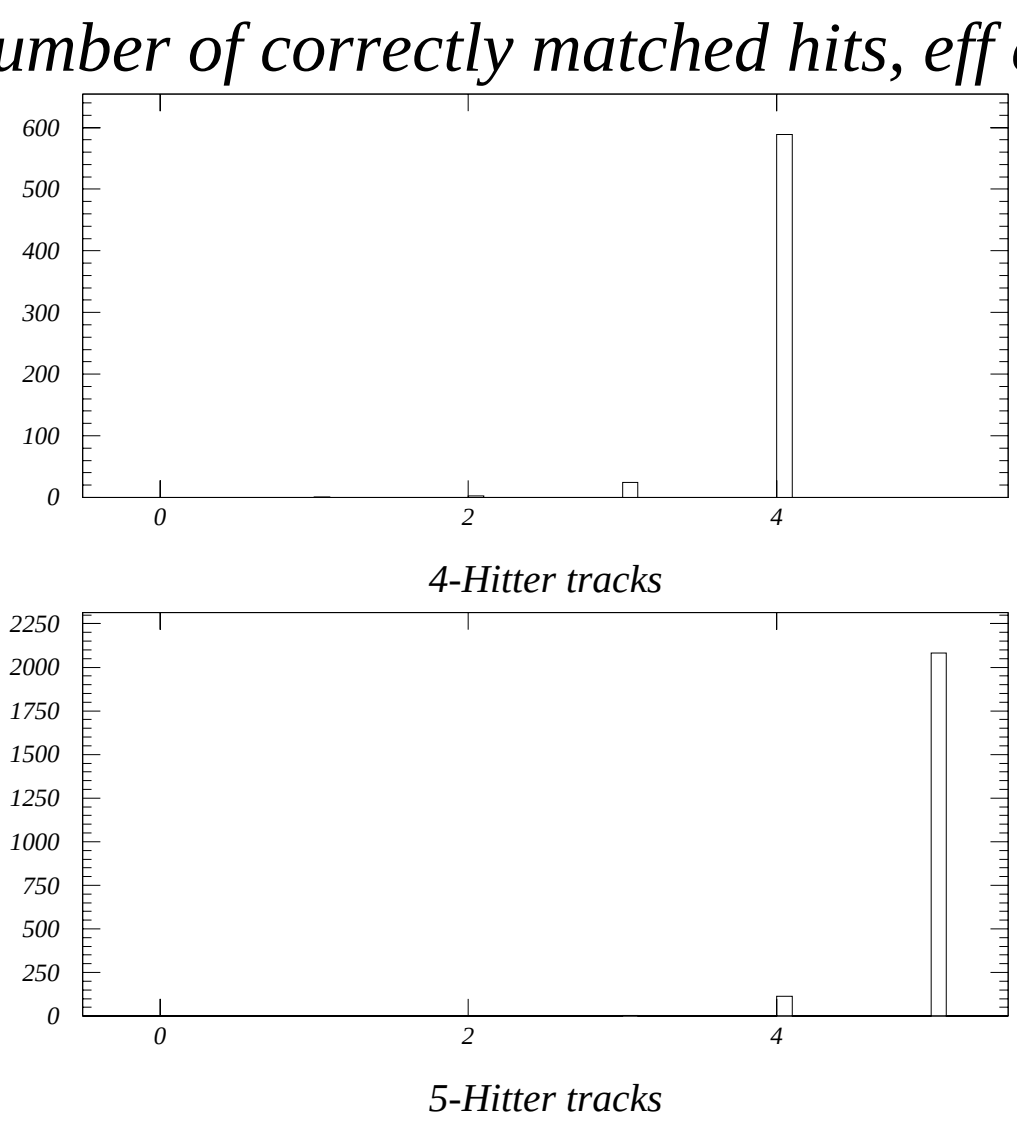


Figure 12: The number of correctly matched hits on SVXII standalone tracks after pruning.

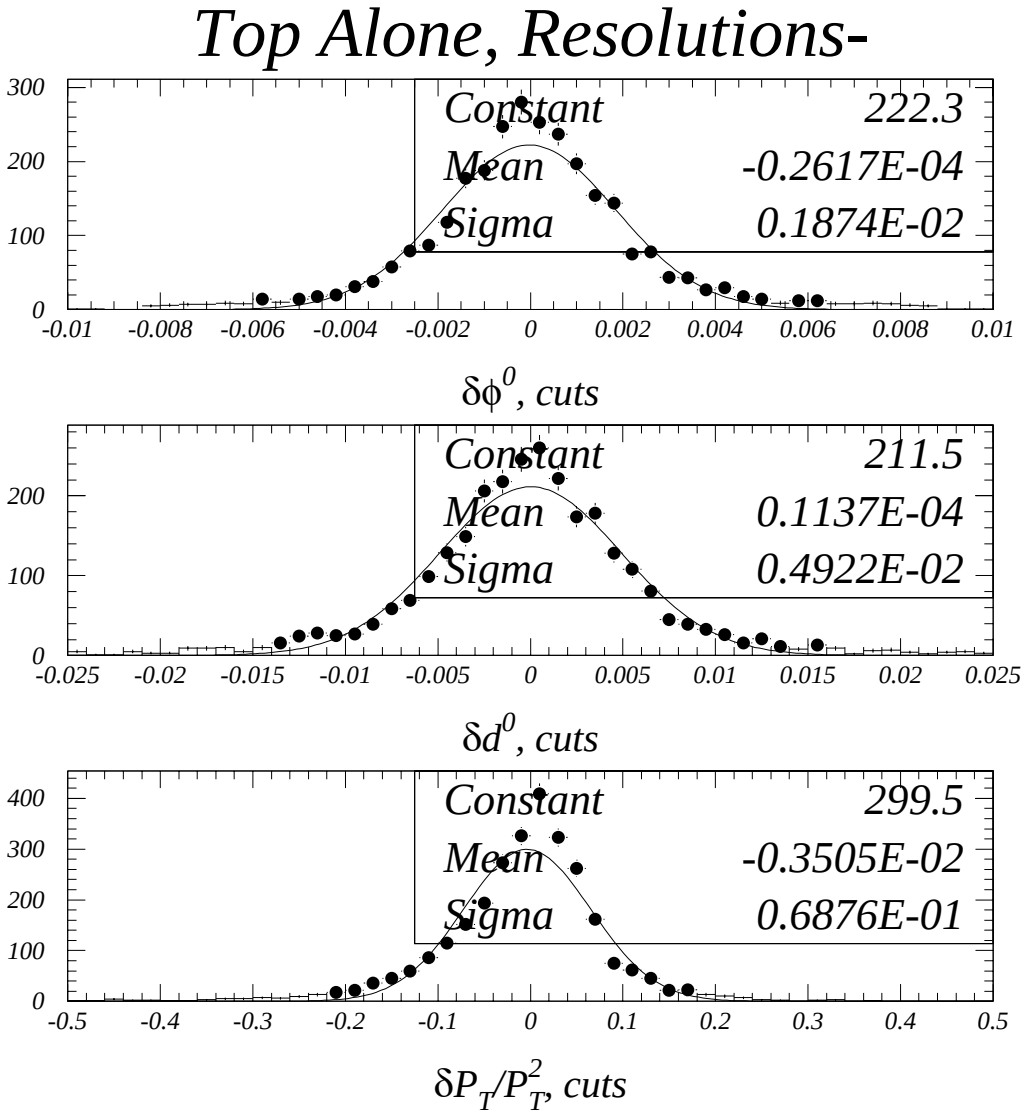


Figure 13: The resolutions obtained with SVXII standalone tracking.

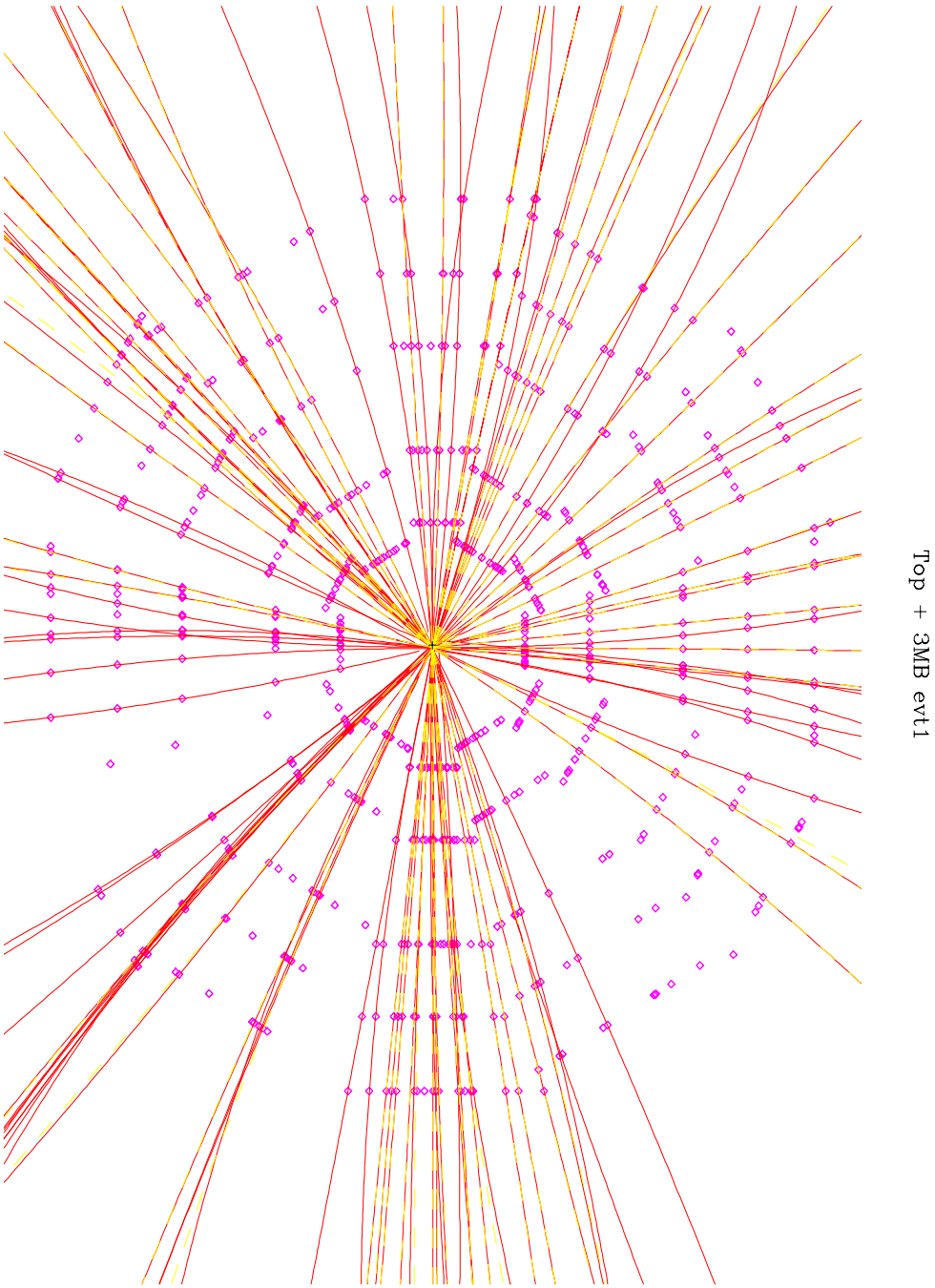


Figure 14: A sample MC top plus 3 min-bias event demonstrates the results of the SVXII standalone tracking. The SVXII hits are shown by the points. The solid red lines show the tracks found by the SVXII standalone tracking and pruning. The dashed yellow lines show the path of the OBS particles. A cut of $p_T > 400$ MeV is applied in both cases, and the unused hits are from particles below 400 MeV.

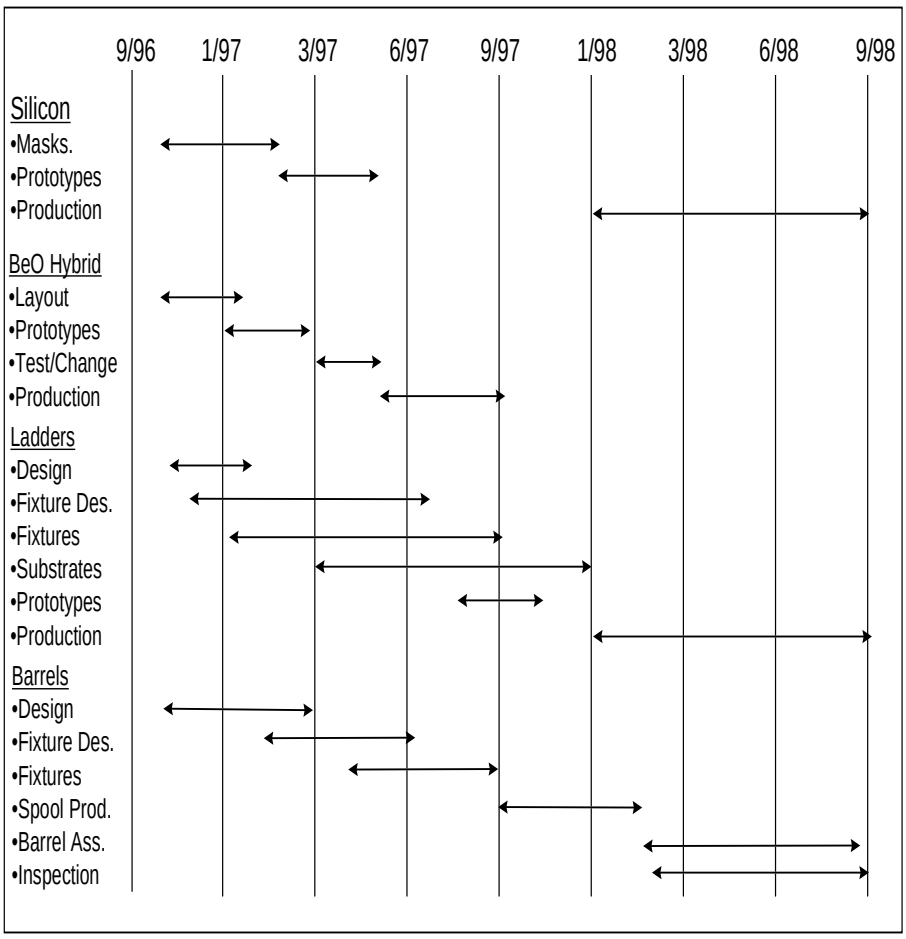


Figure 15: The production schedule.